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09/495,150	01/31/2000	Gopal Hegde	30019.103US01	4464

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EXAMINER
DAY, HERNG DER

ART UNIT	PAPER NUMBER
2123	6

DATE MAILED: 08/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Pg

Office Action Summary	Application No. 09/495,150	Applicant(s) HEGDE ET AL.	
	Examiner Herng-der Day	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This communication is in response to Applicants' Amendment and Response (paper # 5) to Office Action dated February 24, 2003 (paper # 4), mailed May 27, 2003.

1-1. Claims 1, 2, 8, 12, and 14 have been amended; claim 13 has been cancelled; claims 1-12 and 14-17 are pending.

1-2. Claims 1-12 and 14-17 have been examined and claims 1-12 and 14-17 have been rejected.

Drawings

2. The Draftsperson has objected to the drawings; see the copy of Form PTO 948 for an explanation.

Specification

3. The amendment filed May 27, 2003, is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The amended material, which is not supported by the original disclosure, is as follows:

(1) Amended limitation in line 5 of claim 8, as described in page 2 of paper # 5. Claims 8-11 containing the new matter are also rejected under 35 U.S.C. 112, first paragraph, as detailed in section **5-1** below.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 8-11 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

5-1. The amended claim 8 recites the limitation "requesting an access to the hardware model from the software via the network" in line 5 of the claim. However, the original specification, as described in lines 1-2 of page 18, discloses "requesting an access to a hardware model from a hardware side to a software side". The amended limitation does not appear to be supported by the original disclosure. Therefore, claims 8-11 eventually contain subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 8-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7-1. Claim 8 recites the limitation "the bus functional model" in lines 3-4 and 7 of the claim. There is insufficient antecedent basis for this limitation in the claim. For the purpose of claim examination, the Examiner will presume that "the bus functional model" as described in claim 8 refers to "the CPU bus functional model".

7-2. Claims 9-11 are rejected as being dependent on the rejected claim 8.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-5, 7-12, 14-15, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Bauer et al., "Hardware/Software Co-Simulation in a VHDL-based Test Bench Approach", Proceedings of the 34th Design Automation Conference, June 1997, pages 774-779.

9-1. Regarding claim 1, Bauer et al. disclose a method of developing an ASIC using a hardware model, a software, and a network, the hardware model comprising a CPU bus functional model (VHDL design units, page 775, section 3, paragraph 1, comprise; bus functional model, page 777, section 5.2, paragraph 1), the software being coupled to a CPU server, and the network configured to provide communication between the hardware model and the software, the method comprising the steps of:

developing the hardware model and the software concurrently (use the unit under test as a hardware model for the software test; software acts as a generator and analyzer for the unit under test, page 774, section 1, paragraph 4); and

communicating command and control information directly between the CPU server and the CPU bus functional model over the network, and communicating command information directly between the CPU bus functional model and the CPU server over the network to co-simulate the hardware model and the software while the hardware model and the software are being developed (TCP/IP, page 778, section 5.3, paragraphs 7-9).

9-2. Regarding claim 2, Bauer et al. further disclose that the hardware model is developed on a workstation (same host as the VHDL tool, page 778, section 5.3, paragraph 4).

9-3. Regarding claim 3, Bauer et al. further disclose that the software is developed on a target board (test bench, page 778, section 6, paragraphs 2-3).

9-4. Regarding claim 4, Bauer et al. further disclose that the network is a TCP/IP protocol (TCP/IP, page 778, section 5.3, paragraphs 7-8).

9-5. Regarding claim 5, Bauer et al. further disclose that the hardware to be co-simulated is described by a high-level language model (VHDL simulator, page 778, section 5.3, paragraph 9).

9-6. Regarding claim 7, Bauer et al. further disclose receiving test inputs for the co-simulation from a test tool (Traffic Generator, page 779, Figure 3).

9-7. Regarding claim 8, Bauer et al. disclose a method of co-simulating a hardware model and a software in ASIC development, the hardware model comprising a CPU bus functional model, the software being coupled to a CPU server and communicating with the hardware model via a network coupled to the bus functional model and the CPU server, the method comprising:

requesting an access to the hardware model from a hardware side to a software side via the network (software command, page 778, section 5.3, paragraph 6);

invoking a function call by the CPU server (calls the corresponding software routines, page 778, section 5.3, paragraph 6);

sending an access request from the CPU bus functional model to the CPU server via the network (via VHDL communication channels; to TCP/IP link, page 778, section 5.3, paragraph 6);

routing the access request to the hardware model (to the micro processor model, page 778, section 5.3, paragraph 7).

developing the hardware model and the software concurrently; and co-simulating the hardware model and the software while the hardware model and the software are being developed (use the unit under test as a hardware model for the software test; software acts as a generator and analyzer for the unit under test, page 774, section 1, paragraph 4).

9-8. Regarding claim 9, Bauer et al. further disclose that the function call is a READ function call (micro processor command; read operation, page 778, section 5.3, paragraph 7).

9-9. Regarding claim 10, Bauer et al. further disclose that the function call is a WRITE function call (micro processor command; write operation, page 778, section 5.3, paragraph 7).

9-10. Regarding claim 11, Bauer et al. further disclose requesting a hardware model interrupt, and a function call to handle the interrupt being invoked by the software via the network (If an interrupt occurs, an exception handling procedure is called, page 778, section 5.2, paragraph 4).

9-11. Regarding claim 12, Bauer et al. disclose an apparatus for hardware model and software co-simulation in ASIC development comprising:

a hardware model, the hardware model representing a hardware board circuit to be co-simulated/tested (VHDL simulator, page 778, section 5.3, paragraph 9), the hardware model being developed on a workstation and including a CPU bus functional model (same host as the VHDL tool, page 778, section 5.3, paragraph 4; VHDL design units, page 775, section 3, paragraph 1, include; bus functional model, page 777, section 5.2, paragraph 1);

a software, the software providing command and control accesses of the hardware model, the software being developed/debugged on a target board (test bench, page 778, section 6, paragraphs 2-3) concurrently with a design of the hardware model (use the unit under test as a hardware model for the software test; software acts as a generator and analyzer for the unit under test, page 774, section 1, paragraph 4), the target board including a CPU server in communication with the software (an interface module for the software was designed, page 778, section 5.3, paragraph 4); and

a network coupled between the CPU bus functional model and the CPU server to communicate a command from the software to the hardware model and to route contents of the command between the hardware model and the software, thereby providing co-simulation of the hardware model and software (TCP/IP, page 778, section 5.3, paragraphs 7-8).

9-12. Regarding claim 14, Bauer et al. further disclose that the software is loaded on the CPU server (remote host, page 778, section 5.3, paragraph 4).

9-13. Regarding claim 15, Bauer et al. further disclose that the network is a TCP/IP protocol (TCP/IP, page 778, section 5.3, paragraphs 7-8).

9-14. Regarding claim 17, Bauer et al. further disclose that the hardware model is capable of receiving test inputs for co-simulation from a test tool (Traffic Generator, page 779, Figure 3).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bauer et al., "Hardware/Software Co-Simulation in a VHDL-based Test Bench Approach", Proceedings of the 34th Design Automation Conference, June 1997, pages 774-779, in view of Rowson, "Hardware/Software Co-Simulation", Proceedings of the 31st ACM/IEEE Conference on Design Automation Conference, June 1994, pages 439-440.

11-1. Regarding claim 6, Bauer et al. disclose the hardware/software co-simulation in a project consists of four ASICs. However, Bauer et al. fail to expressly disclose receiving test inputs for the co-simulation from a real working environment.

Rowson discloses using hardware in place of a software model, i.e. using an actual part as the model, called by the simulator (page 440, column 1, paragraph 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Bauer et al. to receive test inputs through real hardware ports for the co-simulation from a real working environment to obtain the invention as specified in claim 6 because the inputs from a real working environment help the developer find the most common problems in an early stage of the developing process to save development cost. The purpose to develop ASIC products is to make them useful and marketable in a real working

environment. If the developed ASIC products may not function correctly in a real working environment, co-simulation with inputs from a real working environment will help developers to find and correct problems in an early stage of the developing process to save development cost.

11-2. Regarding claim 16, Bauer et al. disclose the hardware/software co-simulation in a project consists of four ASICs where the hardware model is capable of receiving test inputs from the traffic generator. The purpose of traffic generator is to generate packets, which simulates the traffic compatible with a real working environment and has predetermined characteristics, to test the developed products. Bauer et al. fail to expressly disclose that the hardware model is capable of receiving test inputs for the co-simulation from a real working environment.

Rowson discloses using hardware in place of a software model, i.e. using an actual part as the model, called by the simulator (page 440, column 1, paragraph 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Bauer et al. to receive test inputs through real hardware ports for the co-simulation from a real working environment to obtain the invention as specified in claim 16 because through real hardware ports any hardware model being capable of receiving test inputs from the traffic generator will also be capable of receiving test inputs from a real working environment.

Applicants' Arguments

12. Applicants argue the following:

(1) "Bauer fails to disclose a hardware model that includes a CPU bus functional model, and further fails to disclose a network for providing communication between the CPU bus

functional model and a CPU server that is in communication with the software, as required by claims 1, 8 and 12" (page 5, paper # 5).

(2) "claims 6 and 16 are allowable for at least the reason they are dependent upon an allowable base claim" (page 6, paper # 5).

Response to Arguments

13. Applicants' arguments have been fully considered. They are not persuasive.

13-1. Response to Applicants' argument (1). Bauer et al. disclose that the test bench has a hierarchical structure and the interfaces of the unit under test are classified. "VHDL design units, which we call in this case *applications*, relate to an interface classification" (page 775, section 3, paragraph 1). In other words, the VHDL "Micro processor application" (page 777, Figure 2), which includes a bus functional model, is the interface part of the hardware model. The TCP/IP network provides communication between the software and the unit under test through bus functional model, software link, and software client. Claims 1-5, 7-12, 14-15, and 17 are rejected under 35 U.S.C. 102(b), as detailed in sections **9-1** to **9-14** above.

13-2. Response to Applicants' argument (2). Claims 1 and 12 are not allowable claims yet. Claims 6 and 16 are rejected under 35 U.S.C. 103(a), as detailed in sections **11-1** to **11-2** above.

Conclusion

14. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Herng-der Day whose telephone number is (703) 305-5269. The examiner can normally be reached on 9:00 - 17:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (703) 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Herng-der Day
August 6, 2003

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100